

**REMARKS**

Claims 1 to 20 are currently pending in the present application with claims 10 and 13 having been amended herein. The amendments to the claims do not present new matter.

Claims 1, 5 and 14 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,366,467 to Patel et al. (hereinafter “Patel”) and by Klughart, U.S. Patent No. 6,396,137 (in paragraph three of the Office Action). It is respectfully submitted that neither Patel nor Klughart anticipates the subject matter of claims 1, 5 and 14 for the following reasons.

As regards the anticipation rejections of the claims, to reject a claim under 35 U.S.C. § 102(e), the Office must demonstrate that each and every claim feature is identically described or contained in a single prior art reference. (See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed. Cir. 1991))(emphasis added).

Claim 1 recites an interposer layer including voltage regulator elements, the interposer layer having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked **surface-to-surface** with the exposed surface layer.

As regards the Patel reference, the step-down-converter (SDC) and integrated circuit package disclosed therein is precisely the background art referred to in the specification of the above-identified application, which the present invention is intended to improve upon. In particular, Patel discloses placing the SDC, which regulates the voltage, *adjacent* to the integrated circuit, both of which are situated on top of an interposer (See Patel, Figure 3 in which the SDC is numbered as (302), the integrated circuit as (304) and the interposer as (306)). Thus, in Patel, the interposer itself does not include voltage regulator elements, but merely includes conductive traces, serving as an electrical conduit. See Patel, col. 3, lines 66-67; col. 4, lines 34-35.

Accordingly, Applicants respectfully submit that Patel does not disclose (or suggest) an interposer layer including voltage regulator elements that is adapted to be stacked **surface-to-surface** with the exposed surface layer. Furthermore, in each of the embodiments disclosed in Patel, the interposer layer is much larger in surface area than the integrated circuit die so that Patel also does not disclose (or suggest) an interposer

layer that has surface dimensions approximately matching the exposed surface layer of the integrated circuit die.

For at least these reasons, it is submitted that Patel does not anticipate the subject matter of claim 1.

As claims 5 and 14 recite features analogous to those of claim 1, it is submitted that Patel also does not anticipate the subject matter of these claims.

With regard to the Klughart reference, as discussed in the previously submitted amendment of July 7, 2004, Klughart does not disclose stacking a voltage regulator layer directly *surface-to-surface* with the exposed surface layer of the integrated circuit die, but rather, explicitly provides for a separate insulating layer (2605 of Figure 17) situated between the voltage regulator/switch and the integrated circuit. Accordingly, in Klughart, the layer that includes a voltage regulator is not stacked surface-to-surface with the exposed layer of the integrated circuit die.

Moreover, the positioning of the insulating layer described in Klughart is not merely a matter of design choice since the silicon-on-insulator (SOI) fabrication technique used to produce the structure topology in Klughart ***necessarily produces an insulating layer*** in between the foundation integrated circuit and a conduction routing layer including a power supply. See Klughart, col. 27, line 62 to col. 28, line 11. Thus, Klughart not only does not disclose a surface-to-surface coupling between a voltage regulator and an integrated circuit but actually plainly teaches away from this structure.

For at least these reasons, Klughart does not anticipate the subject matter of independent claim 1.

As claims 5 and 14 recite features analogous to those of claim 1, it is submitted that Klughart also does not anticipate the subject matter of these claims.

Withdrawal of the anticipation rejection of claims 1, 5 and 14 based on either Patel or Klughart is accordingly respectfully requested.

Claims 10-13 have been rejected under 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 6,521,530 to Peters et al. (“Peters”).

Independent claim 10, as amended, recites an interposer having voltage regulator elements that include a minority of linear regulator elements and a majority of switching regulator elements. Peters does not disclose this feature. At most, Peters refers to an interposer that includes “active” elements and capacitors. See Peters, col. 20. There is no specific reference to or suggestion of a voltage regulator having both linear regulator and switching elements, let alone a regulator in which the linear regulator elements

comprise a minority and the switching elements comprise a majority. Accordingly, Peters does not anticipate claim 10 or its dependent claims 11-13.

Claims 2-4, 6-13, and 15-20 have been rejected under 35 U.S.C. § 103(a) as unpatentable over Patel in view of U.S. Patent No. 6,264,475 to Li et al. (“Li”). It is respectfully submitted that the combination of Patel and Li does not render obvious the subject matter of claims 2-4, 6-13 and 15-20.

Establishment of *prima facie* obviousness requires satisfaction of three separate criteria. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

It is submitted that the Li reference fails to cure the deficiencies of the primary Patel reference in that it also does not disclose or suggest an interposer layer including voltage regulator elements having surface dimensions approximately matching the exposed surface layer of the integrated circuit die and being adapted to be stacked surface-to-surface with the exposed surface layer. In contrast, Li merely discloses a resilient interposer that provides improved structural properties but does not include voltage regulator elements.

Accordingly, the combination of Patel and Li fails to disclose or suggest each of the elements of independent claims 1, 5, 10 and 14 and dependent claims 2-4, 6-9, 11-13 and 15-20.

Withdrawal of the obviousness rejection of claims 2-4, 6-13 and 15-20 is accordingly respectfully requested.

Claims 10-13 have been rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 6,262,905 to Zhang et al. (“Zhang”) in view of U.S. Patent No. 6,265,771<sup>1</sup> to Ference et al. (“Ference”). It is respectfully submitted that the combination of Zhang and Ference does not render obvious the subject matter of claims 10-13.

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<sup>1</sup> The Examiner apparently inadvertently referred to the patent number of another cited reference when referring to Ference.

Claim 10 recites an interposer situated between the substrate and the integrated circuit die, the interposer having voltage regulator elements for receiving voltage from the power supply and for down-converting the voltage from the power supply into a regulated voltage. As discussed in the previous response, Ference merely refers to integrating a heat sink into an integrated circuit, and does not mention or refer to an interposer layer including voltage regulator elements as claimed. It is therefore submitted that the combination of Zhang and Ference fails to disclose or suggest each of the elements of independent claim 10 and its dependent claims 11-13.

Withdrawal of the obviousness rejection of claims 10-13 is accordingly respectfully requested.

#### CONCLUSION

All issues having been addressed, it is believed that the present application is in condition for allowance. Prompt reconsideration and allowance of the present application are respectfully requested.

Respectfully submitted,

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